OKI Semiconductor

This version: Aug. 1998

MSM7719-01

Echo Canceler with ADPCM Transcoder

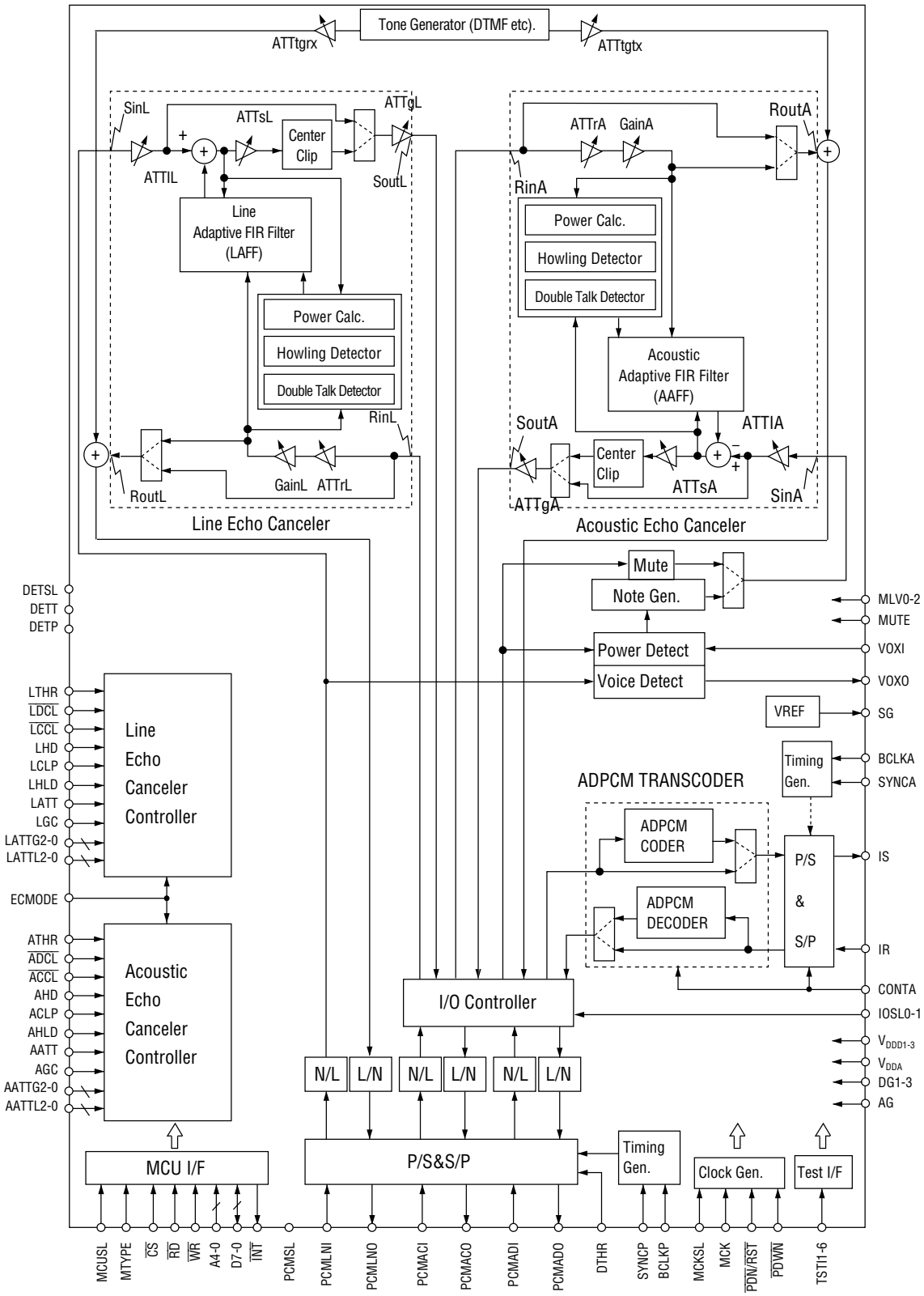
GENERAL DESCRIPTION

The MSM7719, developed for PHS (Personal Handyphone System) applications, is an LSI device and contains a line echo canceler, an acoustic echo canceler (for handsfree conversation), and a single channel full-duplex ADPCM transcoder.
This device includes DTMF tone and several types of tone generation, transmit/receive data mute and gain control, and VOX function and is best suited for PHS applications.

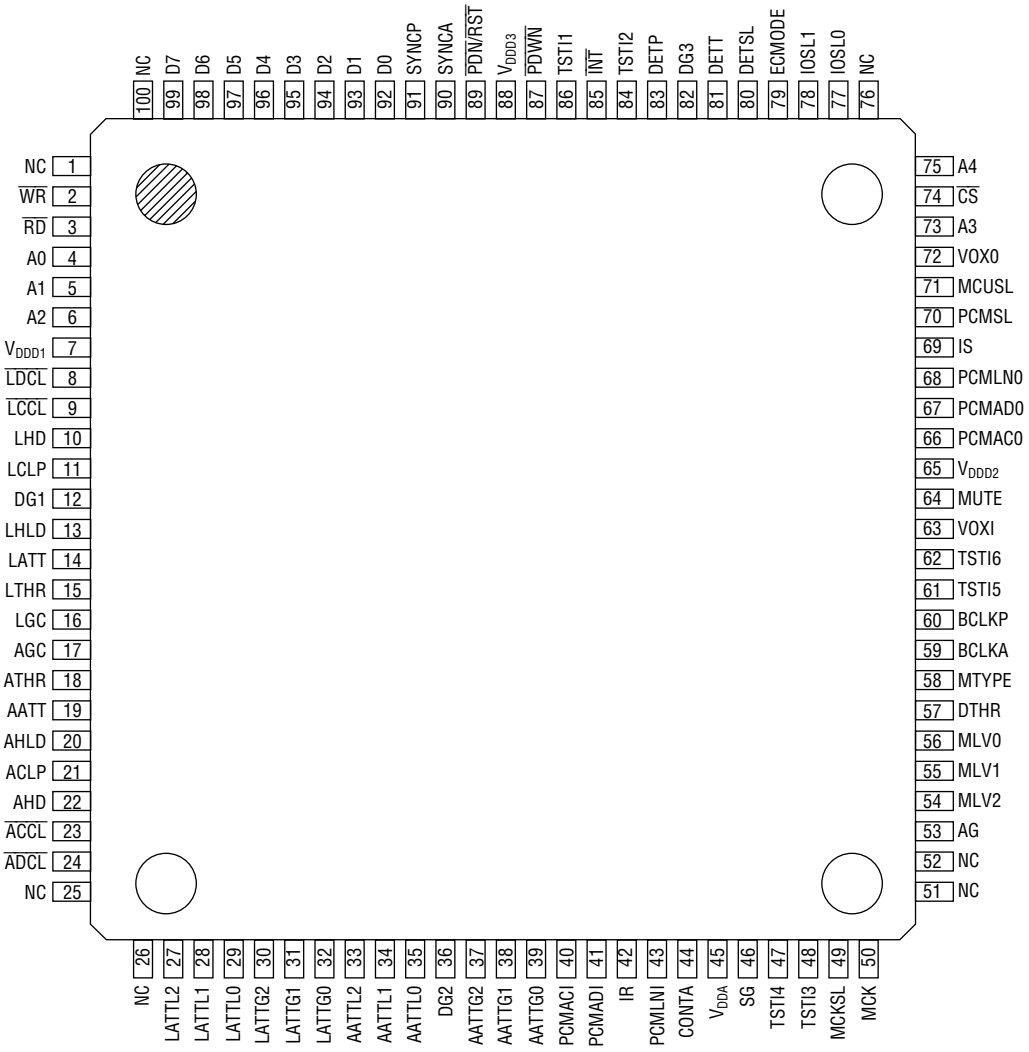
FEATURES

- Single 5 V power supply V_{DD} : 4.5 V to 5.5 V
- ADPCM : ITU-T Recommendations G.726
- PCM interface coding format : μ-law
- Built-in 2-channel (line and acoustic) echo canceler
  - Line echo canceler
  - Acoustic echo canceler (for handsfree conversation)
  - Echo attenuation : 30 dB (typ.)
  - Cancelable echo delay time :
    - 27 ms (max.) for line echo canceler +27 ms (max.) for acoustic echo canceler
    - Line echo canceler mode only : 54 ms (max.)
- Serial PCM/ADPCM transmission data rate : 64 kbps to 2048 kbps
- Low supply current
  - Operating mode : Typically 50 mA (V_{DD} = 5.0 V)
  - Power-down mode : Typically 0.2 mA (V_{DD} = 5.0 V)
- Master clock frequency : 9.6 to 10.0 MHz/19.2 to 20.0 MHz
- Transmit/receive mute, transmit/receive programmable gain control
- Built-in DTMF tone generator and various tones generator
- Control through parallel microcontroller interface
  - Pin control available for line and acoustic echo cancelers
- Built-in VOX control
  - Transmit side : Voice/silence detect
  - Receive side : Background noise generation at the absence of voice signal
- Package:
  100-pin plastic TQFP (TQFP100-P-1414-0.50-K) (Product name : MSM7719-01TS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No-connect pin

100-Pin Plastic TQFP

PIN FUNCTIONAL DESCRIPTION

SG

Outputs of the analog signal ground voltage.
The output voltage is approximately 2.4 V. Connect bypass capacitors of 10 µF and 0.1 µF (ceramic type) between these pins and the AG pin. During power-down, the output changes to 0 V.

AG

Analog ground.

DG1, 2, 3

Digital ground.

V_{DDA}

+5 V power supply for analog circuits.

$V_{DDD1, 2, 3}$

+5 V power supply for digital circuits.

$\overline{PDN}/\overline{RST}$

Power-down reset control input.
A logic "0" makes the LSI device enter a power-down state. At the same time, all control register data are reset to the initial state. Set this pin to a logic "1" during normal operating mode. Since this pin is ORed with CR0-B5 (bit 5 (B5) of control register CR0), set CR0-B5 to logic "0" when using this pin. When this pin control is not used (i.e., when controlling by the control register), set this pin to logic "1".

$\overline{PDWN}$

Power-down control input.
The device changes to the power-down state, and each bit of control register and internal variables of control register are not reset when set to a logic "0". During normal operation, set this pin to logic "1". Since this pin is ORed with CR0-B6 (bit 6 (B6) of control register CR0), set CR0-B6 to logic "0" when using this pin. When this pin control is not used (i.e., when controlling by the control register), set this pin to logic "1".

MCK

Master clock input.
The frequency must be 9.6 to 10.0 MHz/19.2 to 20.0 MHz. The master clock signal is allowed to be asynchronous with SYNCP, SYNCA, BCLKP, and BCLKA.

MCKSL

Master clock selection input.
Set MCKSL to logic "0" when the master clock frequency is 9.6 to 10.0 MHz, and to logic "1" when it is 19.2 to 20.0 MHz.

PCMACO

PCM data output of the echo canceler.
PCM is output from MSB in a sequential order, synchronizing with the rising edge of BCLKP and SYNCP.
This pin is in a high impedance state except during 8-bit PCM output. When DTHR is set to logic "1", this pin becomes a 4-bit output and the input data to the input pin set by IOSL0-1 is output as it is. In this case, this pin is in a high impedance state except during 4-bit output. Note that the echo canceler signal output mode for this pin changes depending on the setting of IOSL0-1. (This pin is also in a high impedance state during power-down or initial mode.)
Refer to Figs. 1-5.

PCMACI

PCM data input of the echo canceler.
PCM is shifted in at the falling edge of BCLKP and input from MSB.
The start of the PCM data (MSB) is identified at the rising edge of SYNCP. When DTHR is set to logic "1", this pin becomes a 4-bit input and the input data is output to the output pin set by IOSL0-1 as it is. This pin is provided with a 500-kΩ pull-up resistor. Note that the echo canceler signal input mode for this pin changes depending on the setting of IOSL0-1.
Refer to Figs. 1-5.

PCMADO

PCM data output.
PCM is serially output from MSB in synchronization with the rising edge of BCLKP and SYNCP. This pin is in a high impedance state except during 8-bit PCM output. When DTHR is set to logic "1", this pin becomes a 4-bit output and the input data to the input pin set by IOSL0-1 is output as it is. In this case, this pin is in a high impedance state except during 4-bit output.
Note that the signal ouput mode for this pin changes and the I/O control signal for this pin switches between BCLKA/SYNCA and BCLKP/SYNCP depending on the setting of IOSL0-1. (This pin is also in a high impedance state during power-down or initial mode.)
Refer to Figs. 1-5.

PCMADI

PCM data input.
PCM is shifted in at the falling edge of the BCLKP signal and input from MSB. The start of the PCM data (MSB) is identified at the rising edge of SYNCP. When DTHR is set to logic "1", this pin becomes a 4-bit input and the input data is output to the output pin set by IOSL0-1 as it is. This pin is provided with a 500-kΩ pull-up resistor. Note that the signal input mode for this pin changes and the I/O control signal for this pin switches between BCLKA/SYNCA and BCLKP/SYNCP depending on the setting of IOSL0-1.
Refer to Figs. 1-5.

IOSL0-1

These pins specify PCM signal I/O mode for the PCMACO, PCMACI, PCMADO, and PCMADI pins. Since The IOSL0 and IOSL1 pins are ORed with the control register bits CR3-B6 and B5, set these bits to logic "0" before using these pins. When this pin control is not used (i.e., in the case of control with the control register), set these pins to logic "0".
Refer to Figs. 1-5.

IS

Transmit ADPCM data output.
This data is serially output from MSB in synchronization with the rising edge of BCLKA and SYNCA. This pin is in a high impedance state except during 4-bit ADPCM output. When CONTA is set to logic "1", this pin becomes an 8-bit output and the data that passed through the ADPCM transcoder is output. In this case, this pin is in a high impedance state except during 8-bit output.
(This pin is also in a high imedance state during power-down or initial mode.)
Refer to Figs. 1-5.

IR

Receive ADPCM data input.
ADPCM is shifted in on the rising edge of BCLKA in synchronization with SYNCA and input data orderly from MSB. When CONTA is set to logic "1", this pin becomes an 8-bit input and the data is passed through the ADPCM transcoder and processed. This pin is provided with a 500-kΩ pull-up resistor.

PCMLNO

PCM receive data output of the line echo canceler.
PCM is output from MSB in a sequential order, synchronizing with the rising edge of BCLKP and SYNCP.
This pin is in a high impedance state except during 8-bit PCM output. When DTHR is set to logic "1", this pin becomes a 4-bit output and the input data to the input pin set by IOSL0-1 is output as it is. In this case, this pin is in a high impedance state except during 4-bit output.
(This pin is also in a high impedance state during power-down or initial mode.)
Refer to Figs. 1-5.

PCMLNI

PCM transmit data input of the line echo canceler.
PCM is shifted in at the falling edge of the BCLKP signal and input from MSB. The start of the PCM data (MSB) is identified at the rising edge of SYNCP. When DTHR is set to logic "1", this pin becomes a 4-bit input and the input data is output to the output pin set by IOSL0-1 as it is. This pin is provided with a 500-kΩ pull-up resistor.
Refer to Figs. 1-5.

BCLKA

Shift clock input for the ADPCM data (IS, IR).
The frequency is from 64 kHz to 2048 kHz.

SYNCA

8 kHz synchronous signal input for ADPCM data.
Synchronize this data with BCLKA signal. SYNCA is used for indicating the MSB of the serial ADPCM data stream.

BCLKP

Shift clock input for the PCM data (PCMLNO/PCMLNI, PCMACO/PCMACI, PCMADO/PCMADI). The frequency is set in the range of 64 kHz to 2048 kHz.

SYNCP

8 kHz synchronous signal input for PCM data.
This signal must be synchronized with the BCLKP signal.

MCUSL, MTYPE

If the microcontroller interface is not to be used, set the MCUSL input pin to logic "1". This setting skips the intitial mode as the operating mode. For the MTYPE pin, which is the microcontroller interface selection pin, logic "0" sets the read/write independent control mode and logic "1" sets read/write shared control mode.
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "0".

$\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$

A 19-byte control register is provided in this LSI device. Data is read and written by using these pins from the external microcontroller. See the microcontroller write and read timing diagrams in the Electrical Characteristics.
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "1".

A4-A0, D7-D0

A4-A0 are address input pins of the control register, and D7-D0 are data I/O pins.
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "0".

$\overline{\text{INT}}$

Reserved.

PCMSL

Reserved.

CONTA

ADPCM transcoder setting pin. When this pin is set to logic "1", the transcoder-through mode is set. In this mode, the IS and IR pins become 8-bit PCM serial input and output pins. Since this pin is ORed with the control register bit CR1-B7, set CR1-B7 to logic "0" to use this pin.
When this pin control is not used (i.e., when controlling by the control register), set this pin to logic "0".
Refer to Figs. 1-5.

DTHR

Through mode setting pin. When this pin is set to logic "1", the entire circuit is put in the through mode. In this mode, the PCM input and output pins become 4-bit serial input and output pins and all functions of the echo canceler, ADPCM transcoder, and MUTEVOX are disabled. Use this pin when making 32-kbps data communication.
Since this pin is ORed with the control register bit CR1-B5, set CR1-B5 to logic "0" to use this pin.
When this pin control is not used (i.e., when controlling by the control register), set this pin to logic "0".
Note that 64-kbps data communication is not supported in this device.
Refer to Figs. 1-5.

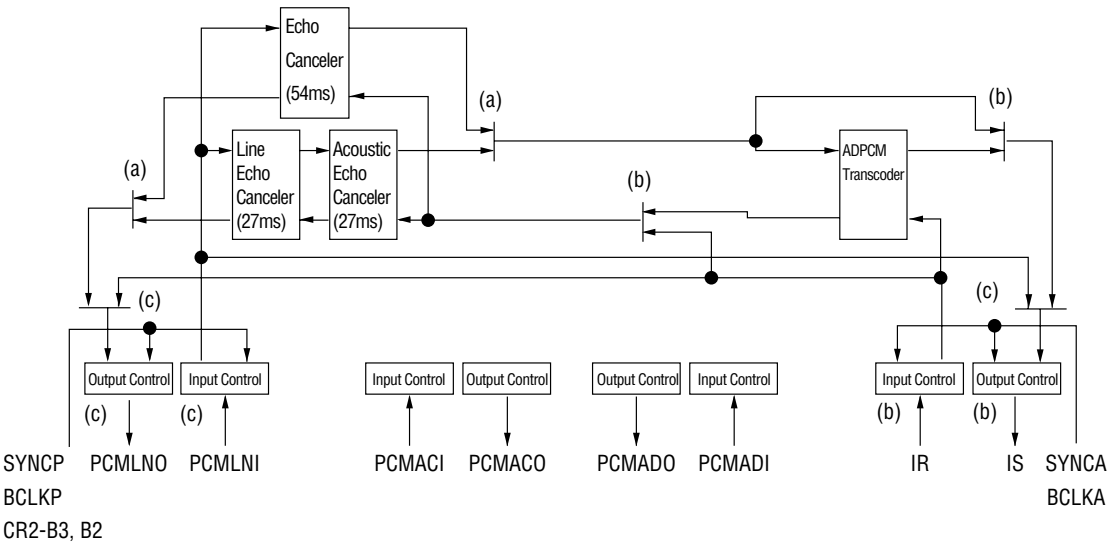


Figure 1 Signal I/O Control 1

IOSL1="0", IOSL0="0"
Control (a): ECMODE, CR0-B0
Control (b): CONTA, CR1-B7
Control (c): DTHR, CR1-B5

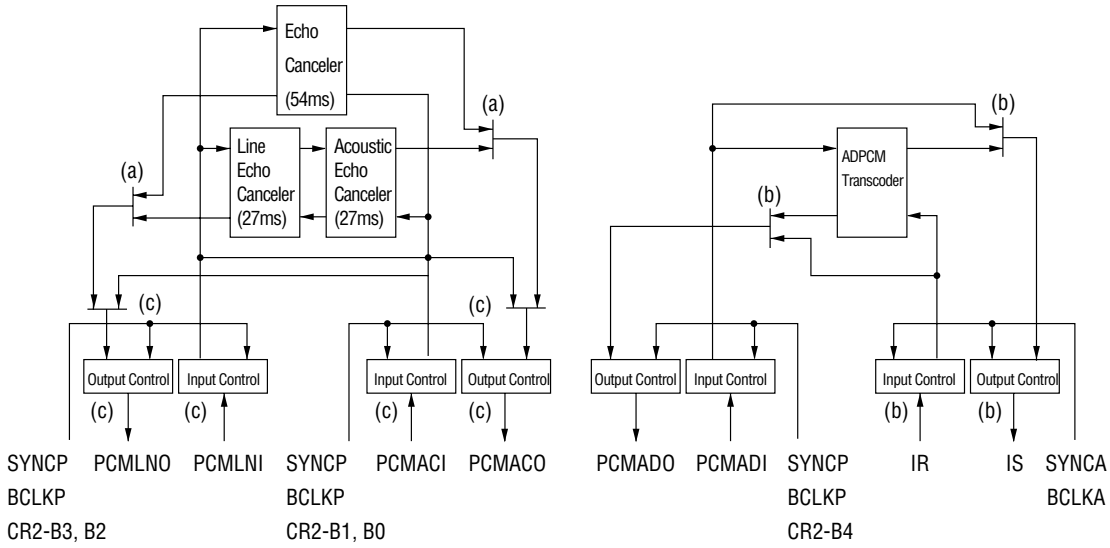


Figure 2 Signal I/O Control 2

IOSL1="0", IOSL0="1"
Control (a): ECMODE, CR0-B0
Control (b): CONTA, CR1-B7
Control (c): DTHR, CR1-B5

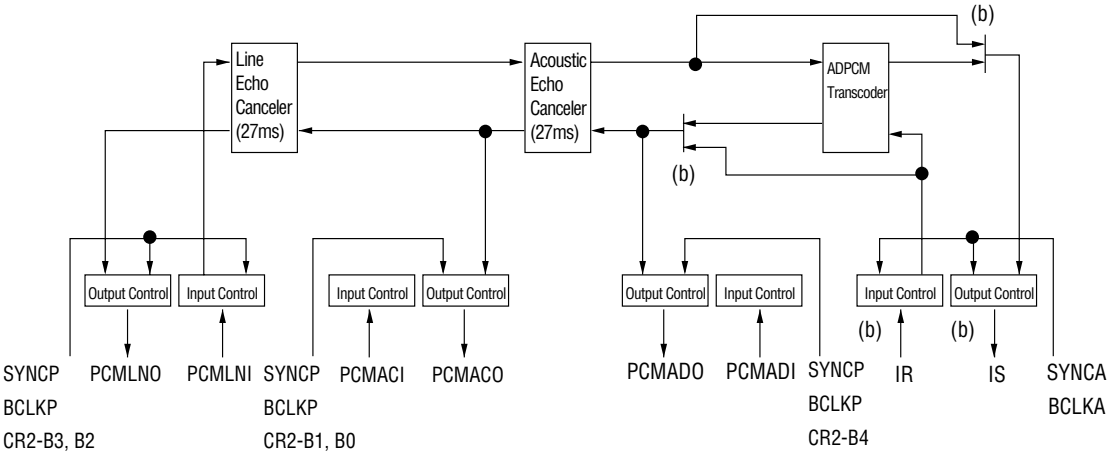


Figure 3 Signal I/O Control 3

IOSL1="1", IOSL0="0"
Control (a): ECMODE, CR0-B0
Control (b): CONTA, CR1-B7
Control (c): DTHR, CR1-B5

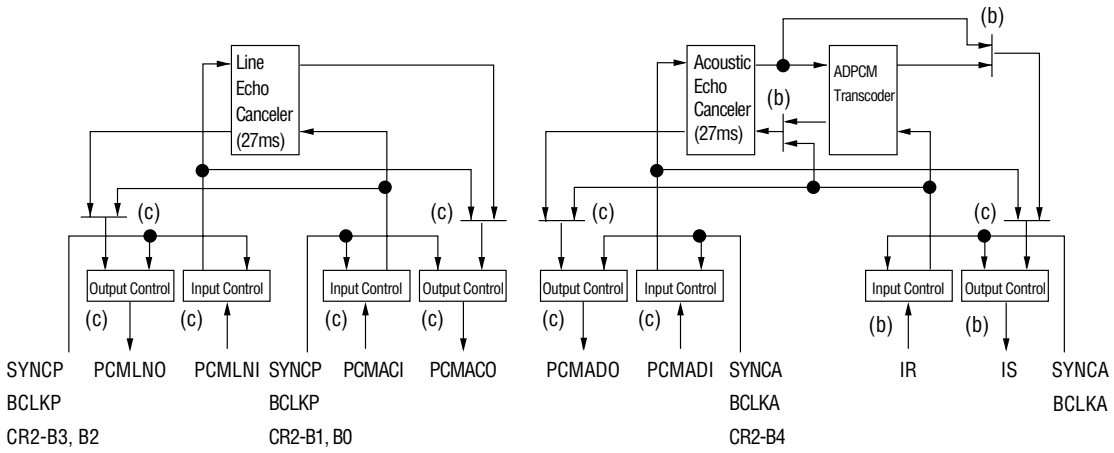
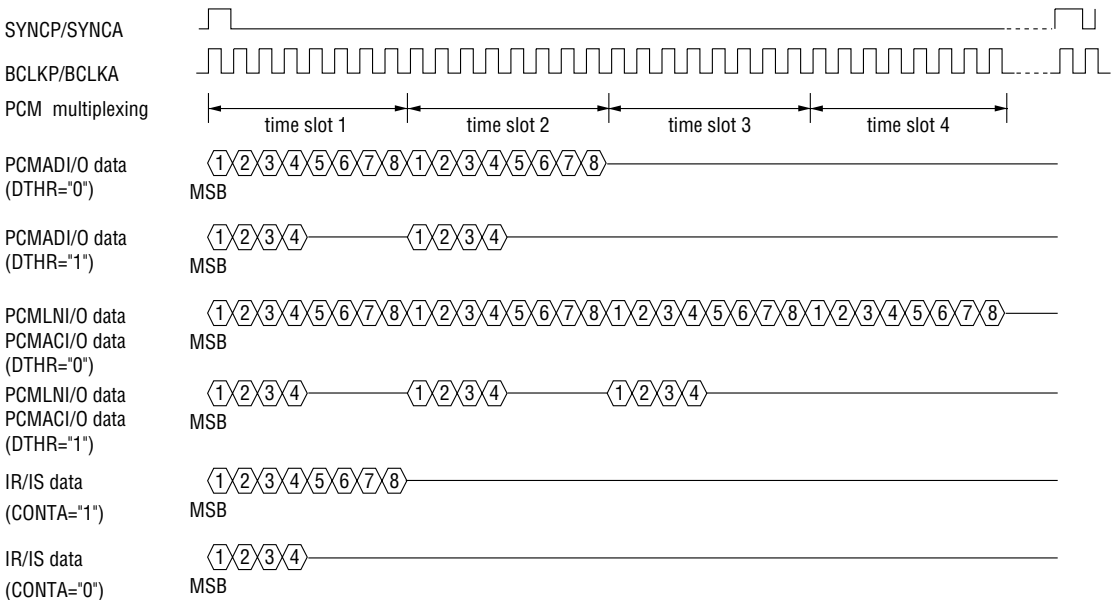


Figure 4 Signal I/O Control 4

IOSL1="1", IOSL0="1"
Control (a): ECMODE, CR0-B0
Control (b): CONTA, CR1-B7
Control (c): DTHR, CR1-B5



Note: The PCM signals (PCMADI and PCMADO) of the ADPCM transcoder can be assigned to time slot 1 or 2.
The PCM signals (PCMLNI, PCMLNO, PCMACI, and PCMACO) of the echo canceler can be assigned to one of the time slots 1 to 4.
The ADPCM signals (IR and IS) of the ADPCM transcoder are always assigned to time slot 1.

Figure 5 PCM Multiplexing/ADPCM Timing

ECMODE

This pin specifies the operating mode of the echo canceler. When set to logic "0", this device operates as a line echo canceler (with cancelable echo delay time of 27 ms max.) + an acoustic echo canceler (with cancelabel echo delay time of 27 ms max.); when set to logic "1", it operates as a line echo canceler (with cancelable echo delay time of 54 ms max.).
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "0".

LTHR, ATHR

(L: Line A: Acoustic)
These pins control the through mode of the echo canceler. In this mode, SinL/A data and RinL/A data is output directly to SoutL/A and RoutL/A respectively, while retaining their echo canceler coefficients.
0: Normal mode (Echo cancellation) 1: Through mode
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "1".

$\overline{\text{LDCL}}$, $\overline{\text{ADCL}}$

These pins control clearing the coefficient 1 of the adaptive FIR filter used by the echo canceler. If the echo path changes, reset both the coefficient 1 (by setting $\overline{\text{LDCL}}$/$\overline{\text{ADCL}}$ to "0") and the coefficient 2 (by setting $\overline{\text{LCCL}}$/$\overline{\text{ACCL}}$ to "0") of the adaptive FIR filter whenever possible.
0: Resets the coefficient 1: Normal operation
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "1".

$\overline{\text{LCCL}}$, $\overline{\text{ACCL}}$

These pins control clearing the coefficient 2 of the adaptive FIR filter used by the echo canceler. If the echo path changes, reset both the coefficient 1 (by setting $\overline{\text{LDCL}}$/$\overline{\text{ADCL}}$ to "0") and the coefficient 2 (by setting $\overline{\text{LCCL}}$/$\overline{\text{ACCL}}$ to "0") of the adaptive FIR filter whenever possible.
0: Resets the coefficient 1: Normal operation
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "1".

LHD, AHD

Howling detection ON/OFF control pins.
0: OFF, 1: ON
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "0".

LCLP, ACLP

These pins turn ON or OFF the Center Clipping funciton that forcibly sets the SoutL output of the line echo canceler to minimum positive value when it is –57 dBm0 or less.
0: Center Clipping OFF
1: Center Clipping ON
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "0".

LHLD, AHLD

These pins control updating the coefficient of the adaptive FIR filter (AFF) for the echo canceler.
0: Normal mode (updates the coefficient)
1: Coefficient Fixed mode
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "0".

LATT, AATT

These pins turn ON or OFF the ATT function that prevents howling from occurring by means of attenuators ATTsL/A and ATTrL/A provided for the RinL/A input and the SoutL/A output of the echo canceler.
When a signal is input to RinL/A only, the attenuator ATTsL/A of the SoutL/A output is activated. When a signal is input to SinL/A only or to both SinL/A and RinL/A, the attenuator ATTrL/A of the RinL/A input is activated. The ATT values are both about 6 dB.
0: ATT function ON
1: ATT function OFF
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "0".

LGC, AGC

These pins turn ON or OFF the gain control function that controls the RinL/A input level and prevents howling from occurring by the gain controller (GainL/A) provided for the RinL/A input of the echo canceler. The RinL/A input level is adjusted in the attenuation range of 0 to –8.5 dB. This adjusting starts at the RinL/A input level of –24 dBm0.
0: gain control OFF
1: gain control ON
When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "0".

MUTE

Receive side voice path mute level enable pin. To set a mute level, set this pin to logic "1".
When this pin control is not used (i.e., when controlling by the control register), set this pin to logic "0".

MLV0-2

Receive side voice path mute level setting pins. For the control method, refer to the control register (CR1) description. Since this signal is ORed with CR1-B2, B1, and B0 internally, set the bits of the register to logic "0" before using these pins.

DETSL

Reserved pin.
Set this pin to logic "0".

DETT

Reserved pin.
Set this pin to logic "0".

DETP

Reserved pin.
Set this pin to logic "0".

LATTG2-0, AATTG2-0

Pad setting pins for the echo canceler's SoutL/A output gain.

Level	ATTG2	ATTG1	ATTG0
0 dB	0	0	0
2 dB	0	0	1
4 dB	0	1	0
6 dB	0	1	1
8 dB	1	0	0
10 dB	1	0	1
12 dB	1	1	0
14 dB	1	1	1

When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "0".

LATTL2-0, AATTL2-0

Pad setting pins for the echo canceler's SinL/A input loss.

Level	ATTL2	ATTL1	ATTL0
–0 dB	0	0	0
–2 dB	0	0	1
–4 dB	0	1	0
–6 dB	0	1	1
–8 dB	1	0	0
–10 dB	1	0	1
–12 dB	1	1	0
–14 dB	1	1	1

When this pin control is not used (i.e., when controlling by the control register), set these pins to logic "0".

TSTI1-6

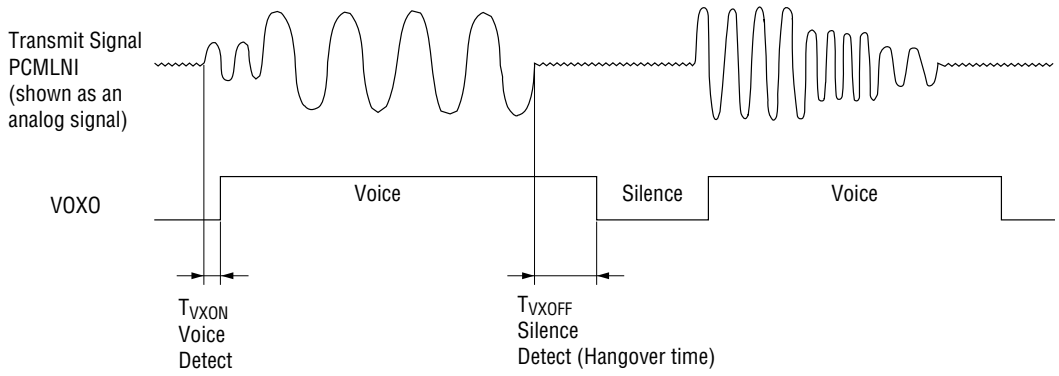
Test input pins.
Tie to logic "0".

VOXO

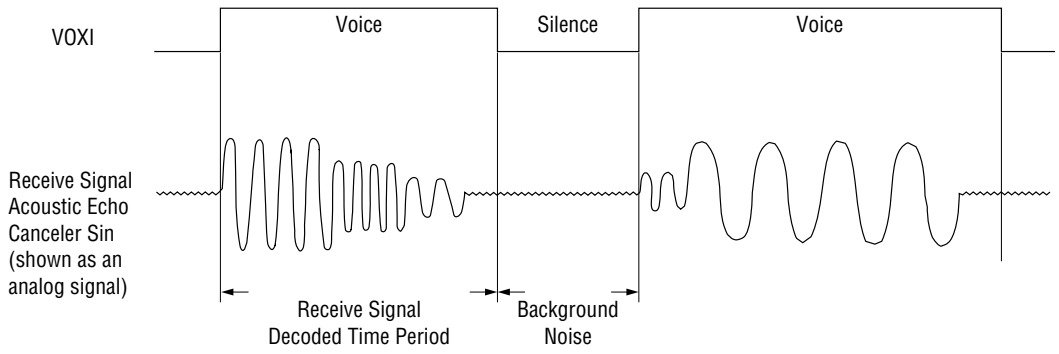
Signal outut for transmit side VOX function.
This pin is effective when CR6-B7 is set to logic "1" (VOX ON).
The VOX function recognizes the presence or absence of the transmit voice signal by detecting the level of the transmit signal to the line echo canceler. "1" and "0" levels set to this pin correspond to the presence and the absence of voice, respectively. This result appears also at the register bit CR7-B7. The signal energy detect threshold is set by the control register bits CR6-B6, B5.
The timing diagram of the VOX function is shown in Figure 3.
The transmit signal to the line echo canceler refers to the signal input to the PCMLNI pin.
Refer to Figure 6.

VOXI

Signal input for receive side (acoustic echo canceler Sin side) VOX function.
The "1" level at VOXI indicates the presence of a voice signal, the decoder block processes normal receive signal, and the voice signal on the PCMACI pin goes through. The "0" level indicates the absence of a voice signal and the background noise generated in this device is output.
The background noise amplitude is set by the control register CR6.
Because this signal is ORed with the register bit CR6-B3, set CR6-B3 to logic "0" when using this pin.
When this pin control is not used (i.e., when controlling by the control register), set this pin to logic "0".
Refer to Figure 6.



(a) Transmit Side VOX Function Timing Diagram



(b) Receive Side VOX Function Timing Diagram

Figure 6 VOX Function

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +7.0	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Digital Output Voltage	V_{OUT}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	+4.5	—	+5.5	V
Operating Temperature	Ta	—	–25	+25	+70	°C
Input High Voltage	V_{IH}	All digital inputs	2.4	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	All digital inputs	0	—	0.8	V
Digital Input Rise Time	t_{Ir}	All digital inputs	—	—	5	ns
Digital Input Fall Time	t_{If}	Measurement point=0.8V&2.4V	—	—	5	ns
Master Clock Frequency	f_{MCK}	MCK (When MCKSL="1")	–100 ppm	19.2-20.0	+100 ppm	MHz
		MCK (When MCKSL="0")		9.6-10.0		
Master Clock Duty Ratio	D_C	MCK	40	50	60	%
Bit Clock Frequency	f_{BCK}	BCLKP, BCLKA	64	—	2048	kHz
Synchronous Pulse Frequency (*1)	f_{SYNC}	SYNCP, SYNCA	—	8.0	—	kHz
Clock Duty Cycle (*2)	D_{CK}	BCLKP, BCLKA	40	50	60	%
Transmit Sync Pulse Setting Time	t_{XS}	BCLKP to SYNCP, BCLKA to SYNCA	100	—	—	ns
	t_{SX}	SYNCP to BCLKP, SYNCA to BCLKA	100	—	—	ns
	t_{XO}	SYNCP to BCLKP, SYNCA to BCLKA	—	—	100	ns
Receive Sync Pulse Setting Time	t_{RS}	BCLKP to SYNCP, BCLKA to SYNCA	100	—	—	ns
	t_{SR}	SYNCP to BCLKP, SYNCA to BCLKA	100	—	—	ns
	t_{RO}	SYNCP to BCLKP, SYNCA to BCLKA	—	—	100	ns
Receive Sync Pulse Setting Time	t_{WS}	SYNCP, SYNCA	1 BCLK	—	100	µs
PCM, ADPCM Set-up Time	t_{DS}	—	100	—	—	ns
PCM, ADPCM Hold Time	t_{DH}	—	100	—	—	ns

*1 If SYNCP and SYNCA are generated from different clocks, be sure to keep the relative timing of the rising edges of SYNCP and SYNCA (that is, which rising edge is earlier) after releasing the reset.

*2 The recommended condition (values) for the clock duty cycle need not be observed if the clock duty cycle fulfills the digital interface timing.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 to 5.5 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current 1	I_{DD1}	Operating mode, no signal (V_{DD}=5 V)	—	50	80	mA
Power Supply Current 2	I_{DD2}	Power down mode (V_{DD}=5 V, only the master clock is input)	—	0.2	1	mA
Input Leakage current	I_{IL}	V_I= V_{DD}	–10	—	+10	µA
High Level Digital Output Voltage	V_{OH}	I_{OH}= –0.4 nA	4.2	—	V_{DD}	V
Low Level Digital Output Voltage	V_{OL}	I_{OL}=3.2 mA	0	0.2	0.4	V
Digital Output Leakage Current	I_{LO}	V_I=V_{DD}/0 V	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF

Analog Interface Characteristics

(V_{DD} = 4.5 to 5.5 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SG Output Voltage	V_{SG}	SG	2.35	2.4	2.45	V
SG Output Impedance	R_{SG}	SG	—	40	80	kΩ

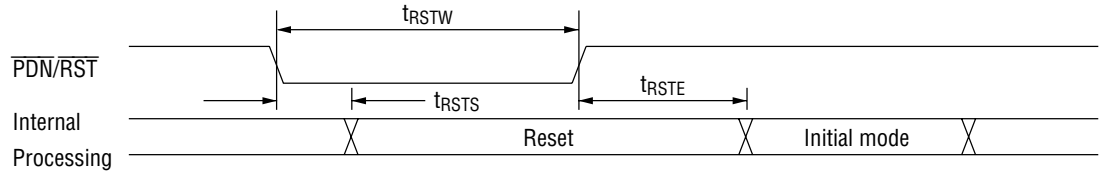
Reset Timing

(V_{DD} = 4.5 to 5.5 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset Signal Width	t_{RSTW}	—	1	—	—	µs
Reset Start Time	t_{RSTS}	—	—	—	1	µs
Reset Termination Time	t_{RSTE}	—	—	—	200	ms

Note: Values in the table are common to the $\overline{PDN}$/$\overline{RST}$ pin and the control register bit CR0-B5.

• Reset timing



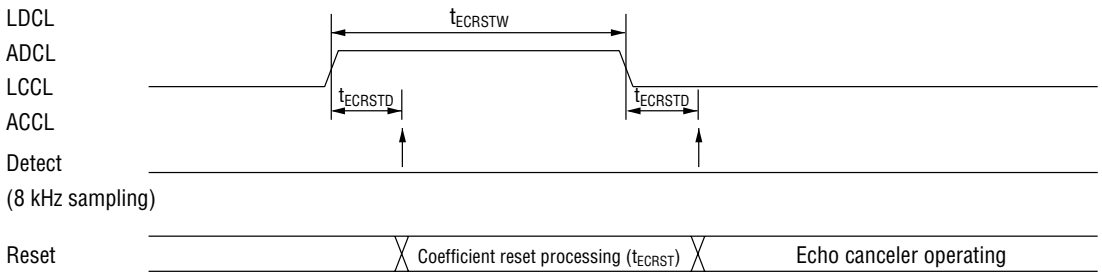
Echo Canceler Coefficient Reset Timing

(V_{DD} = 4.5 to 5.5 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo Canceler Reset Signal Width	t_{ECRSTW}	—	125	—	—	µs
Echo Canceler Reset Detection Time	t_{ECRSTD}	—	0	—	125	µs
Echo Canceler Reset Operating Time	t_{ECRST}	—	—	—	125	µs

Note: Values in the table are common to the $\overline{PDN}/\overline{RST}$ pin and the control register bit CR0-B5.

• Echo canceler coefficient reset timing



Note : In the above timing, the LDCL, ADCL, LCCL, and ACCL register bits are active high, and the $\overline{LDCL}$, $\overline{ADCL}$, $\overline{LCCL}$, and $\overline{ACCL}$ pins are active low.

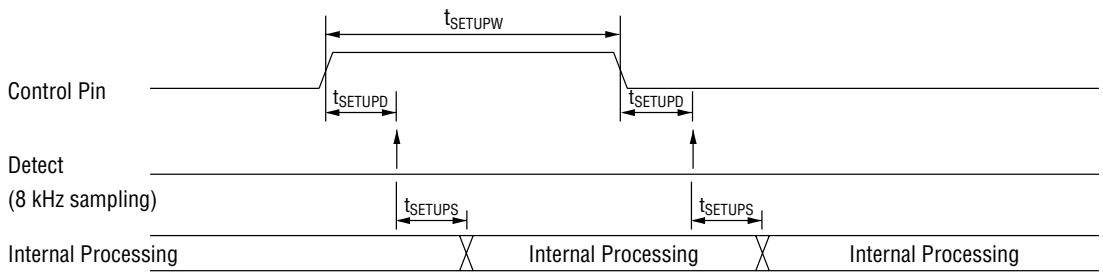
Control Pin Timing

(V_{DD} = 4.5 to 5.5 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Control Signal Width	t_{SETUPW}	—	125	—	—	µs
Control Signal Detection Time	t_{SETUPD}	—	0	—	125	µs
Operation Start Time	t_{SETUPS}	—	0	—	125	µs

Note: The control pins / register bits are as follows:
DETSL, DETT, DETP, (A/L)THR, (A/L)DCL, (A/L)CCL, (A/L)HLD, (A/L)ATT, (A/L) GC, (A/L)ATTG2-0, (A/L)ATTL2-0, PCMSL, DTHR, IOSL0-1, CINTA, MUTE, MLV0-2

• Control pin timing

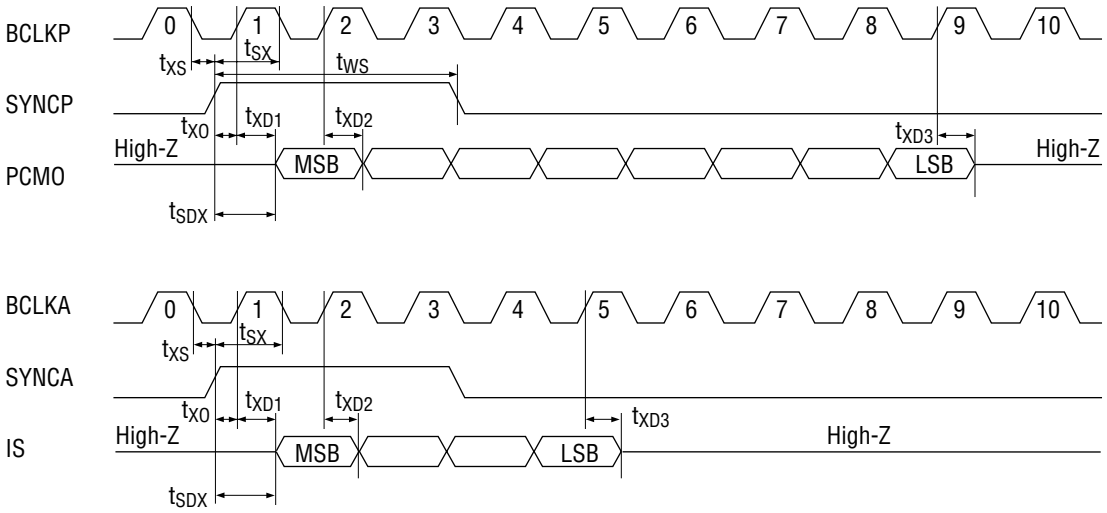


Digital Interface Characteristics

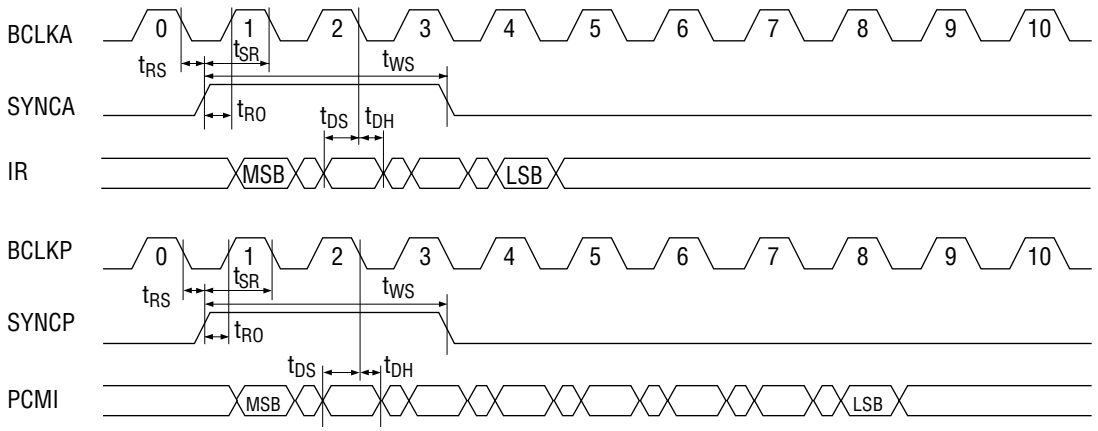
(V_{DD} = 4.5 to 5.5 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital Output Delay Time	t_{SDX}, t_{SDR}	—	0	—	100	ns
PCM, ADPCM Interface	t_{XD1}, t_{RD1}		0	—	100	ns
	t_{XD2}, t_{RD2}		0	—	100	ns
	t_{XD3}, t_{RD3}		0	—	100	ns

• PCM/ADPCM output timing



• PCM/ADPCM input timing



AC Characteristics (Gain Settings)

(V_{DD} = 4.5 to 5.5 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/Receive Gain Setting Accuracy	D_G	For all gain set values	–1	0	+1	dB

AC Characteristics (VOX Function)

(V_{DD} = 4.5 to 5.5 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Transmit VOX Detection Time	t_{VXON}	Silence→voice	VOXO pin:see Fig.6 Voice/silence differential:10 dB	—	5	—	ms
(Voice Signal ON/OFF Detect Time)	t_{VXOFF}	Voice→silence		140/300	160/320	180/340	ms
Transmit VOX Detection Level Accuracy (Voice Detection Level)	D_{VX}	For detection level set values by CR6-B6,B5		–2.5	0	+2.5	dB

AC Characteristics (DTMF and Other Tones)

(V_{DD} = 2.7 to 3.6 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Frequency Deviation	Df_{T1}	DTMF Tones		–1.5	—	+1.5	%
	Df_{T2}	Other various tones		–1.5	—	+1.5	%
Tone Reference Output Level (*1)	V_{TL}	Transmit side tone (Gain set value:0dB)	DTMF (Low group)	–10	–8	–6	dBm0
	V_{TH}		DTMF (High group), Others	–8	–6	–4	dBm0
	V_{RL}	Receive side tone (Gain set value:0dB)	DTMF (Low group)	–10	–8	–6	dBm0
	V_{RH}		DTMF (High group), Others	–8	–6	–4	dBm0
Relative Value of DTMF Tones	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		1	2	3	dB

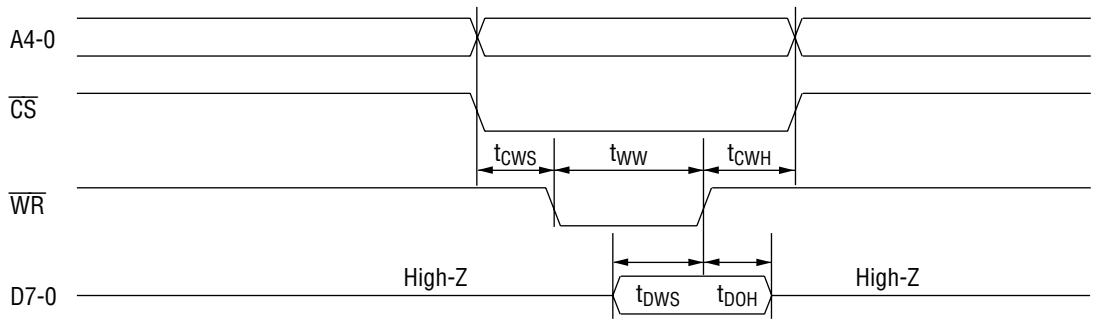
*1 Not including programmable gain set values

Microcontroller Interface ($\overline{WR}$ and $\overline{RD}$ Pins Controlled Independently)

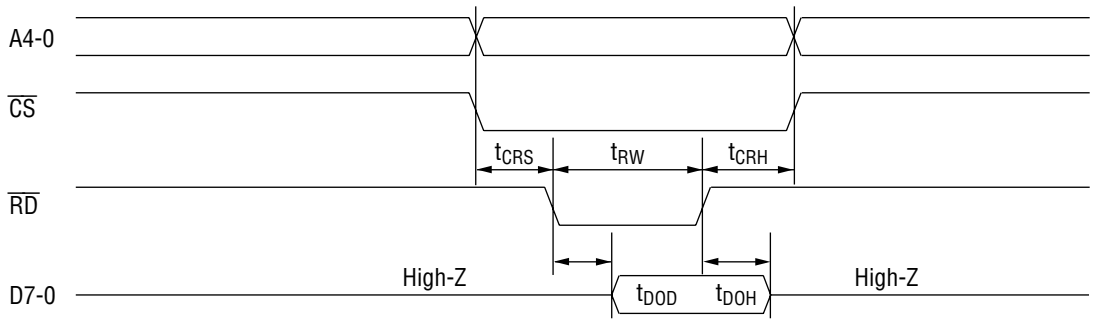
(V_{DD} = 4.5 to 5.5 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address and Chip Select Setup Time (with respect to the falling edge of $\overline{WR}$)	t_{CWS}	MTYPE=0	30	—	—	ns
Address and Chip Select Setup Time (with respect to the rising edge of $\overline{WR}$)	t_{CWH}		15	—	—	
$\overline{WR}$ Pulse Width	t_{WW}		45	—	—	
Data Input Setup Time	t_{DWS}		30	—	—	
Data Input Hold Time	t_{DWH}		15	—	—	
Address and Chip Select Setup Time (with respect to the falling edge of $\overline{RD}$)	t_{CRS}		30	—	—	
Address and Chip Select Setup Time (with respect to the rising edge of $\overline{RD}$)	t_{CRH}		15	—	—	
$\overline{RD}$ Pulse Width	t_{RW}		45	—	—	
Data Output Setup Time	t_{DOD}		—	—	40	
Data Output Hold Time	t_{DOH}		0	—	—	

• Microcontroller write timing ($\overline{WR}$ and $\overline{RD}$ controlled independently)



• Microcontroller read timing ($\overline{WR}$ and $\overline{RD}$ controlled independently)

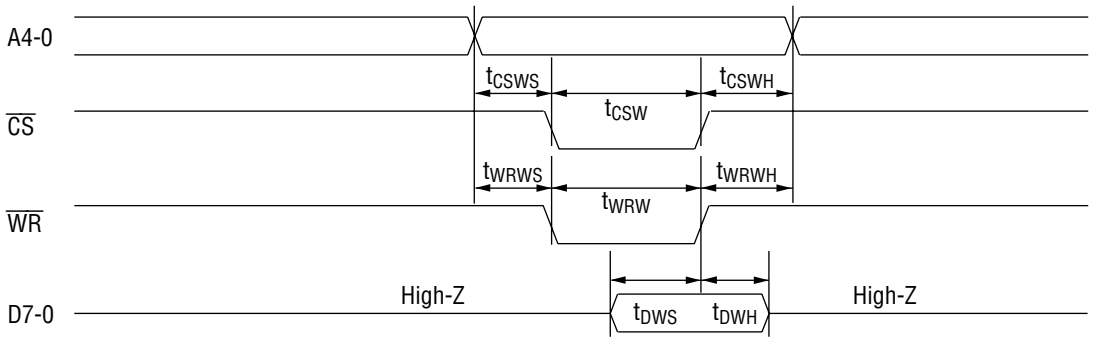


Microcontroller Interface (Shared Control of $\overline{WR}$ and $\overline{RD}$ Pins)

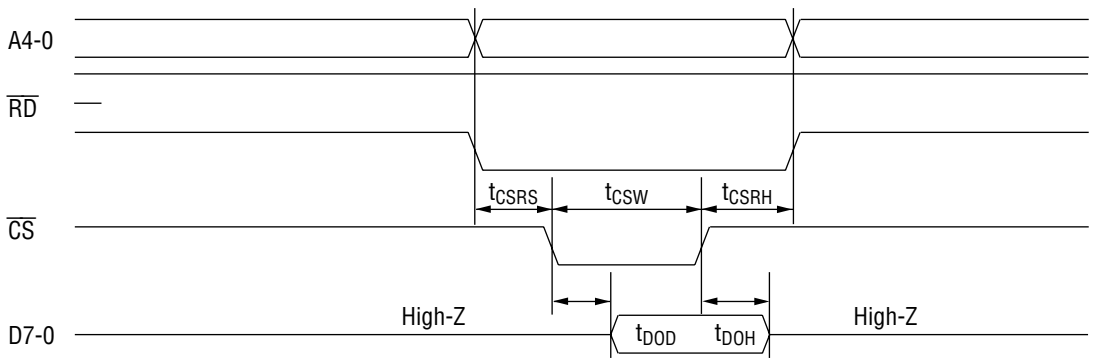
(V_{DD} = 4.5 to 5.5 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address Setup Time (with respect to the falling edge of $\overline{WR}$)	t_{WRWS}	MTYPE=1	30	—	—	ns
Address Setup Time (with respect to the rising edge of $\overline{WR}$)	t_{WRWH}		15	—	—	
$\overline{WR}$ Pulse Width	t_{WRW}		45	—	—	
Address Setup Time (with respect to the falling edge of $\overline{CS}$)	t_{CSWS}		30	—	—	
Address Setup Time (with respect to the rising edge of $\overline{CS}$)	t_{CSWH}		15	—	—	
$\overline{CS}$ Pulse width	t_{CSW}		45	—	—	
Data Input Setup Time	t_{DWS}		30	—	—	
Data Input Hold Time	t_{DWH}		15	—	—	
Address Setup Time (with respect to the falling edge of $\overline{CS}$)	t_{CSRS}		30	—	—	
Address Setup Time (with respect to the rising edge of $\overline{CS}$)	t_{CSRH}		15	—	—	
Data Output Delay Time	t_{DOD}		—	—	40	
Data Output Hold Time	t_{DOH}		0	—	—	

• Microcontroller write timing (shared control of $\overline{WR}$ and $\overline{RD}$)

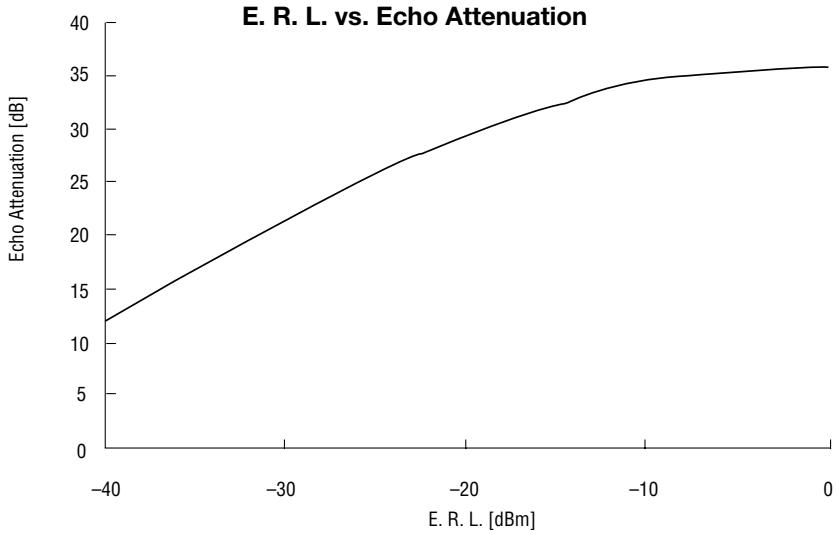


• Microcontroller read timing (shared control of $\overline{WR}$ and $\overline{RD}$)



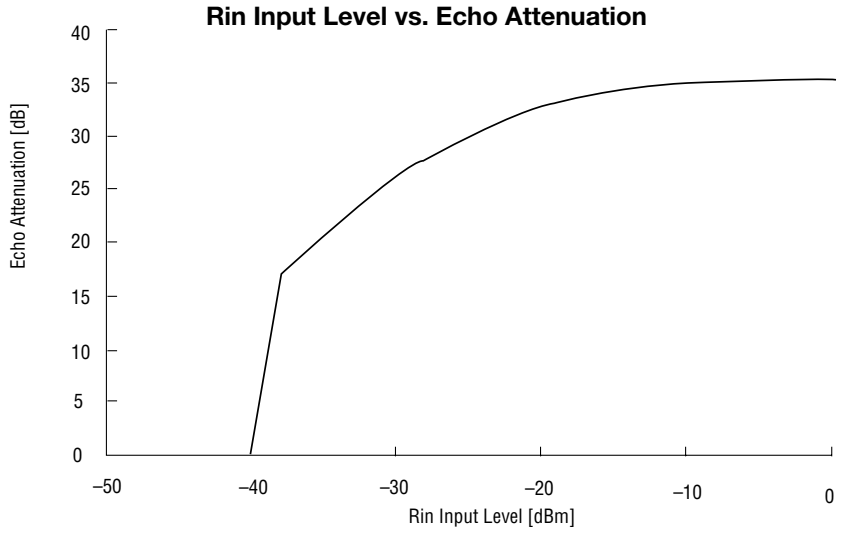
Echo return loss (E. R. L.) vs. echo attenuation

Conditions:
- Input level of white noise of –10 dBm, 3.4 kHz band at Rin
- Echo delay time: 2 ms
- ATT, GC, NLP: Off



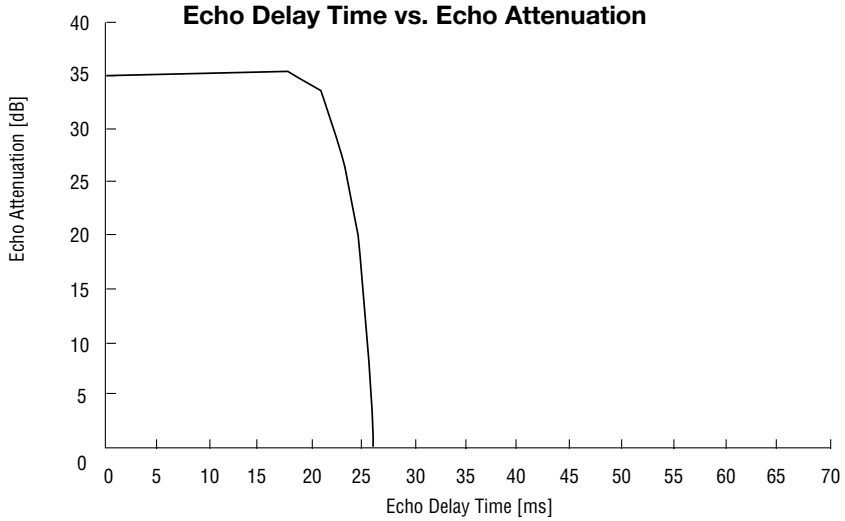
Rin input vs. echo attenuation

Conditions:
- Input level of 3.4 kHz-band white noise at Rin
- Echo delay time: 2 ms
  E. R. L.=–6 dBm
- ATT, GC, NLP: Off

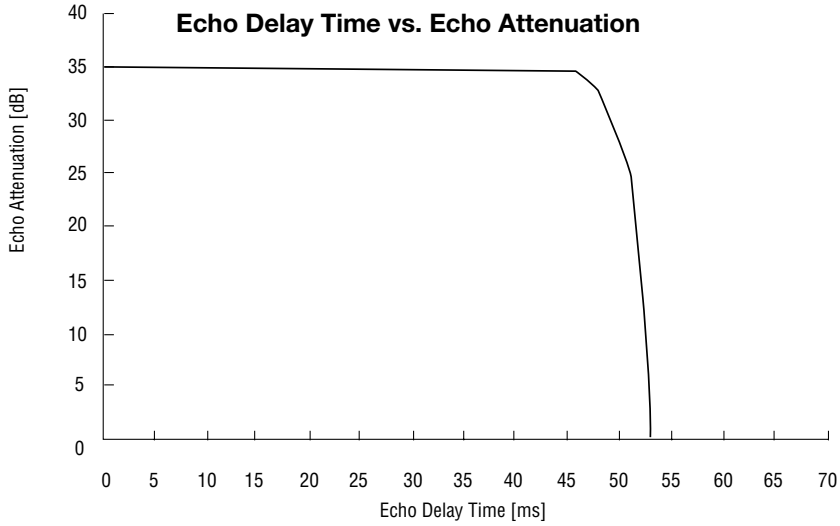


Echo delay time vs. echo attenuation

Conditions:
- Input level of white noise of –10 dBm, 3.4 kHz band at Rin
  E. R. L.= –6 dBm
- ATT, GC, NLP: Off
  ECMODE=27 ms



Conditions:
- Input level of white noise of –10 dBm, 3.4 kHz band at Rin
  E. R. L.= –6 dBm
- ATT, GC, NLP: Off
  ECMODE=54 ms



FUNCTIONAL DESCRIPTION

Control Registers

Table 1 Control Register Map

Reg Name	Address					Contents								R/W
	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	0	0	—	PDWN	PDN/ RST	—	OPE MODE3	OPE MODE2	OPE MODE1	OPE MODE0	R/W
CR1	0	0	0	0	1	CONTA	ADPCM RESET	DTHR	TX MUTE	RX MUTE	RX MLV2	RX MLV1	RX MLV0	R/W
CR2	0	0	0	1	0	—	—	—	PCM AD SEL	PCM LN SEL1	PCM LN SEL0	PCM AC SEL1	PCM AC SEL0	R/W
CR3	0	0	0	1	1	PCMSL	IOSL1	IOSL0	—	DETSL	DETAUTO	DETT	DETP	R/W
CR4	0	0	1	0	0	TX TONE GAIN3	TX TONE GAIN2	TX TONE GAIN1	TX TONE GAIN0	RX TONE GAIN3	RX TONE GAIN2	RX TONE GAIN1	RX TONE GAIN0	R/W
CR5	0	0	1	0	1	DTMF/OTHERS SEL	TX TONE SEND	RX TONE SEND	TONE4	TONE3	TONE2	TONE1	TONE0	R/W
CR6	0	0	1	1	0	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX. NOISE LEVEL SEL	RX. NOISE LVL1	RX. NOISE LVL0	R/W
CR7	0	0	1	1	1	VOX OUT	Silence Level 1	Silence Level 0	INT	DET CPT	DET DTMF	DETL	DETA	R
CR8	0	1	0	0	0	LTHR	LDCL	LCCL	LHD	LCLP (NLP)*	LHLD (ADP)*	LATT (ATT)*	LGC (GC)*	R/W
CR9	0	1	0	0	1	ATHR	ADCL	ACCL	AHD	ACLP (NLP)*	AHLD (APD)*	AATT (ATT)*	AGC (GC)*	R/W
CR10	0	1	0	1	0	—	—	—	DMWR	D TONE3	D TONE2	D TONE1	D TONE0	R/W
CR11	0	1	0	1	1	LATTL2	LATTL1	LATTL0	LATTG2	LATTG1	LATTG0	—	—	R/W
CR12	0	1	1	0	0	AATTL2	AATTL1	AATTL0	AATTG2	AATTG1	AATTG0	—	—	R/W
CR13	0	1	1	0	1	A15	A14	A13	A12	A11	A10	A9	A8	R/W
CR14	0	1	1	1	0	A7	A6	A5	A4	A3	A2	A1	A0	R/W
CR15	0	1	1	1	1	D15	D14	D13	D12	D11	D10	D9	D8	R/W
CR16	1	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	R/W
CR17	1	0	0	0	1	—	—	—	—	—	—	—	—	R/W
CR18	1	0	0	1	0	—	—	—	—	—	—	—	—	R/W

R/W : Read/Write enable R : Read only register

* : These are the symbols of control pins used in the MSM7602 (echo canceler LSI device).

(1) CR0 (Basic operating mode settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	—	PDWN	PDN/RST	—	OPE MODE3	OPE MODE2	OPE MODE1	OPE MODE0
Initial value *	0	0	0	0	0	0	0	0

* : Indicates the value to be set when a resetting is made through the $\overline{\text{PDN}}/\overline{\text{RST}}$ pin. (Also when reset by bit 5 (B5, PDN/RST), the other bits of CR0 are reset to initial values.)

B7 … Not used
B6 … Power-down (entire system) 0: Power-on 1: Power-down
ORed with the inverted external power-down signals
Set the $\overline{\text{PDWN}}$ pin to "1" when this register is used. The control registers and their internal variables are retained.
B5 … Power-down reset (entire system) 0: Power-on 1: Power-down reset
ORed with the inverted external power-down reset signals
Set the $\overline{\text{PDN}}/\overline{\text{RST}}$ pin to "1" when this register is used. The control registers and their internal variables are reset.
B4 … Not used
B3, 2, 1, 0 … Selection of an operating mode
(0, 0, 0, 0) : Initial mode
This mode enables a change (see Fig. 5) in memory that contains internal default values such as tone generation frequencies.
In this mode, the PCM output pin acts to output idle patterns and the PCM input pin acts to input idle patterns; the echo canceler and the ADPCM transcoder do not operate. When power-down reset occurs or when power-down is released, the device enters the initial mode about 200 ms after that. When the MCUSL pin is set to "1", this mode is skipped. This mode is released by setting any of the following modes:

(0, 1, 0, 0) : Handsfree conversation mode
The tone detector, the ADPCM encoder/decoder, the tone generator, the line echo canceler, and the acoustic echo canceler become operative and can be controlled by the contents of the control registers.

(0, 1, 0, 1) : Line echo canceler expansion mode
The tone detector, the ADPCM encoder/decoder, the tone generator, and the line echo canceler (54 ms) become operative and can be controlled according to the contents of the control registers.

(Others): Not used

This register is internally processed by a logical OR of the MCUSL pin and B2, and between the ECMODE pin and B0.

(2) CR1 (Setting of ADPCM operating mode and PCM I/O signals)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	CONTA	ADPCM RESET	DTHR	TX MUTE	RX MUTE	RX MLV2	RX MLV1	RX MLV0
Initial value	0	0	0	0	0	0	0	0

B7 … Control of through mode for the ADPCM CODEC
0: Normal mode 1: Through mode
This bit is valid when the CONTA pin is set to "0".

B6 … Transmitter/receiver ADPCM resetting (conforming to G.721) 1: Reset

B5 … Control of through mode for transmit/receive signal (4-bit) through the entire circuit
0: Normal mode 1: Through mode
When set to "1", the device enters the through mode for 4-bit transmit/receive signal through the entire circuit, and the PCM input and output pins are configured to be 4-bit serial input and output. All the functions of the echo canceler, ADPCM transcoder, MUTE, and VOX become invalid. Use this bit when making 32-kbps data communication. Note that 64-kbps data communication is not supported in this device.

B4 … Muting of transmitter ADPCM data 1: Mute

B3 … Muting of receiver ADPCM data 1: Muting specified by bits B2, B1, and B0 is enabled.
This bit is valid when the MUTE pin is set to "0".

B2, B1, B0… Setting of a receiver voice path mute level

(MLV2, MLV1, MLV0) =	(0, 0, 0) :	Through
	(0, 0, 1) :	– 6 dB
	(0, 1, 0) :	–12 dB
	(0, 1, 1) :	–18 dB
	(1, 0, 0) :	–24 dB
	(1, 0, 1) :	–30 dB
	(1, 1, 0) :	–36 dB
	(1, 1, 1) :	MUTE

(3) CR2 (Setting of PCM I/O multiplex control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	—	—	—	PCM AD SEL	PCM LN SEL1	PCM LN SEL0	PCM AC SEL1	PCM AC SEL0
Initial value	0	0	0	0	0	0	0	0

B7, 6, 5… Not used

B4 … PCM I/O multiplex timing control (PCMADI and PCMADO pins) of the ADPCM transcoder.
0: Time Slot 1 1: Time Slot 2

B3, 2 … PCM I/O multiplex timing control (PCMLNI, PCMLNO pins) of the line echo canceler (See Table 2.)

B1, 0 … PCM I/O multiplex timing control (PCMACI and PCMACO pins) of the acoustic echo canceler (See Table 2.)

Table 2 PCM Multiplex Timing Control Table

B3 (B1	B2 B0)	Corresponding time slot
0	0	1
0	1	2
1	0	3
1	1	4

Note : The outputs are all in high impedance state for all time slots from the time a resetting is made to the initial mode.

(4) CR3 (Setting of PCM signal I/O)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	PCMSL	IOSL1	IOSL0	—	DETSL	DETAUTO	DETT	DETP
Initial value	0	0	0	0	0	0	0	0

B7 … Reserved
B6, 5 … PCM signal I/O control (see Figs. 1 to 4)
B4 … Not used
B3, 2, 1, 0… Reserved

(5) CR4 (Adjustment of tone generator gain)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	TX TONE GAIN3	TX TONE GAIN2	TX TONE GAIN1	TX TONE GAIN0	RX TONE GAIN3	RX TONE GAIN2	RX TONE GAIN1	RX TONE GAIN0
Initial value	0	0	0	0	0	0	0	0

B7, 6, 5, 4 ... Transmit side gain adjustment for the tone generator [ATTtgtx] (See Table 3.)
B3, 2, 1, 0 ... Receive side gain adjustment for the tone generator [ATTtgrx] (See Table 4.)

Table 3 Setting of Transmit Side Gain of Tone Generator

B7	B6	B5	B4	Tone generator gain	B7	B6	B5	B4	Tone generator gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

Table 4 Setting of Receive Side Gain of Tone Generator

B3	B2	B1	B0	Tone generator gain	B3	B2	B1	B0	Tone generator gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

Settings of Table 4 are made in relation to the following tone levels:
DTMF tone (Low frequency group) : –2 dBm0
DTMF tone (High frequency group) and other tone : 0 dBm0
For example, when bits B3, B2, B1, and B0 are set to "1, 1, 1, 1" (–6 dB), the PCMLNO pin outputs a tone of the following levels:
DTMF tone (Low frequency group) : –8 dBm0
DTMF tone (High frequency group) and other tone : –6 dBm0

The default value change command enables the gain adjustment by –1 dB step.
Writing "390Ah" into the address 16Dh adds a gain of –1 dB to the values in the above table. The default value is "4000h".

(6) CR5 (Setting of tone generator operating mode and tone frequency)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	DTMF/OTHERS SEL	TX TONE SEND	RX TONE SEND	TONE4	TONE3	TONE2	TONE1	TONE0
Initial value	0	0	0	0	0	0	0	0

B7 … Selection of DTMF signal and S stone
0: Others 1: DTMF signal
B6 … Transmission of transmit side tone 0: Not transmit 1: Transmit
B5 … Transmission of receive side tone 0: Not transmit 1: Transmit
B4, 3, 2, 1, 0… Setting of a tone frequency (See Table 5.)

Table 5 Setting of Tone Generator Frequencies

(a) When B7 = "1" (DTMF tone)

B4	B3	B2	B1	B0	Description	B4	B3	B2	B1	B0	Description
*	0	0	0	0	697 Hz + 1209 Hz (1)	*	1	0	0	0	852 Hz + 1209 Hz (7)
*	0	0	0	1	697 Hz + 1336 Hz (2)	*	1	0	0	1	852 Hz + 1336 Hz (8)
*	0	0	1	0	697 Hz + 1477 Hz (3)	*	1	0	1	0	852 Hz + 1477 Hz (9)
*	0	0	1	1	697 Hz + 1633 Hz (A)	*	1	0	1	1	852 Hz + 1633 Hz (C)
*	0	1	0	0	770 Hz + 1209 Hz (4)	*	1	1	0	0	941 Hz + 1209 Hz (*)
*	0	1	0	1	770 Hz + 1336 Hz (5)	*	1	1	0	1	941 Hz + 1336 Hz (0)
*	0	1	1	0	770 Hz + 1477 Hz (6)	*	1	1	1	0	941 Hz + 1477 Hz (#)
*	0	1	1	1	770 Hz + 1633 Hz (B)	*	1	1	1	1	941 Hz + 1633 Hz (D)

(b) When B7 = "0" (Others)
The table below lists default frequencies. Eight tones from "10000" to "10111" are single tones. For procedures to change frequencies, see the next page.

B4	B3	B2	B1	B0	Description	B4	B3	B2	B1	B0	Description
0	0	0	0	0	—	1	0	0	0	0	400 Hz Single tone
0	0	0	0	0	—	1	0	0	0	1	1000 Hz Single tone
0	0	0	1	0	—	1	0	0	0	1	2000 Hz Single tone
0	0	0	1	1	—	1	0	0	1	1	2667 Hz Single tone
0	0	1	0	0	—	1	0	1	0	0	1300 Hz Single tone
0	0	1	0	1	—	1	0	1	0	1	2080 Hz Single tone
0	0	1	1	0	—	1	0	1	1	0	*Hz Single tone
0	0	1	1	1	—	1	0	1	1	1	*Hz Single tone
0	1	0	0	0	—	1	1	0	0	0	—
0	1	0	0	1	—	1	1	0	0	1	—
0	1	0	1	0	—	1	1	0	1	0	—
0	1	0	1	1	—	1	1	0	1	1	—
0	1	1	0	0	—	1	1	1	0	0	—
0	1	1	0	1	—	1	1	1	0	1	—
0	1	1	1	0	—	1	1	1	1	0	—
0	1	1	1	1	—	1	1	1	1	1	—

* User specified frequency (see Table 6)

Frequencies of tones (other than DTMF signals) to be generated by the tone generator can be changed. Tone frequencies can be changed in the Initial mode. See Figure 8 for procedures to change tone frequencies. The related subaddresses are shown below.

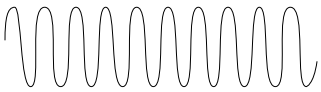
Note: Transmitted Tone Frequency = A × 8.192 (A = frequency)
ex. When frequency = 1000 Hz, 1000 × 8.192 = 9011.2 = 9011d (eliminate after the decimal point) = 2333h

Table 6 Tone Generator Subaddresses

Single tone

B4	B3	B2	B1	B0	Subaddress 1 (Frequency 1) (See Note above)
1	0	0	0	0	178h
1	0	0	0	1	179h
1	0	0	1	0	17Ah
1	0	0	1	1	17Bh
1	0	1	0	0	17Ch
1	0	1	0	1	17Dh
1	0	1	1	0	17Eh
1	0	1	1	1	17Fh

Transmit single tone



(7) CR6 (VOX function control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX. NOISE LEVEL SEL	RX. NOISE LVL1	RX. NOISE LVL0
Initial value	0	0	0	0	0	0	0	0

B7 … Turns ON or OFF the VOX function 0: OFF, 1: ON

B6,5 …Setting of transmit side voice or silence detection level

(0, 0) : –20 dBm0
(0, 1) : –25 dBm0
(1, 0) : –30 dBm0
(1, 1) : –35 dBm0

Note: • The detection level is changeable by inserting the pad of –1dB to –5dB in addion to the alove values.

• Write $16384 \times 10^{(-A/20)}$ at address "2DEh".
Example: When –1dB pad is inserted, $16384 \times 10^{(-(-1)/20)}$
=18383.15=18383d (eliminate after the decimal point)=47CFh

B4 … Setting of hangover time (T_{VXOFF}) (See Figure 6.)
0: 160 ms 1: 320 ms

B3 … VOX input signal (receiver side)
0: Transmits an internal background noise.
1: Transmits a voice reception signal.
Set the VOXI pin to "0" to use this data.

B2 … Setting of a receiver side background noise level
0: Reserved

B1, 0… Externally-set background noise level
(0, 0) : No noise
(0, 1) : –55 dBm0
(1, 0) : –45 dBm0
(1, 1) : –35 dBm0

(8) CR7 (Detection register : read-only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	VOX OUT	Silence level 1	Silence level 0	INT	DET CPT	DET DTMF	DETL	DETA
Initial value	0	0	0	0	0	0	0	0

B7… Detection of transmit side voice or noise
0: Silence 1: Voice

B6, 5… Transmit side silence level (Indicator)
(0, 0) : –10dB or less with respect to the detection level defined by CR6-B6, B5.
(0, 1) : –5 to –10 dB with respect to the detection level defined by CR6-B6, B5.
(1, 0) : –0 to –5 dB with respect to the detection level defined by CR6-B6, B5.
(1, 1) : –0 dB or more with respect to the detection level defined by CR6-B6, B5.
Note : The above outputs are valid only when the VOX function is enabled by bit 7 of CR6.

B4, 3, 2, 1, 0 … Reserved

(9) CR8 (Setting of line echo canceler operating mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR8	LTHR	LDCL	LCCL	LHD	LCLP (NLP)*1	LHLD (ADP)*1	LATT (ATT)*1	LGC (GC)*1
Initial value	1	0	0	0	0	0	0	0

*1 Name of a control pin used by the MSM7602

B7 … Through mode control bit for the line echo canceler
In this mode, RinL data and SinL data is output directly to RoutL and SoutL respectively. The coefficient is not cleared.
1: Through mode 0: Normal mode (echo cancellation)

B6 … Selects whether or not to clear the coefficient 1 of the adaptive FIR filter (LAFF) used by the line echo canceler.
1: Resets the coefficient
0: Normal operation

B5 … Selects whether or not to clear the coefficient 2 of the adaptive FIR filter (LAFF) used by the line echo canceler.
1: Resets the coefficient
0: Normal operation

B4 … Howling detector (HD) ON/OFF control 1: ON 0: OFF

B3 … Turns ON or OFF the Center Clipping function which forcibly sets the SoutL output of the line echo canceler to minimum positive value when it is –57 dBm0 or less.
1: Center Clipping ON
0: Center Clipping OFF

B2 … Selects whether or not to update the coefficient of the adaptive FIR filter (LAFF) for the line echo canceler.
1: Coefficient Fixed mode
0: Normal mode (updates the coefficient.)

B1 … Turns ON or OFF the ATT function which prevents howling from occurring by means of attenuators ATTsL and ATTrL provided for the RinL input and the SoutL output of the line echo canceler.
When a signal is input to RinL only, the attenuator ATTsL of the SoutL output is activated. When a signal is input to SinL only or to both SinL and RinL, the attenuator ATTrL of the RinL input is activated. Their ATT values are both about 6 dB.
1: ATT function OFF
0: ATT function ON

B0 … Turns ON or OFF the gain control function which controls the RinL input level and prevents howling from occurring by the gain controller (GainL) for the RinL input of the line echo canceler.
The RinL/A input level is adjusted in the attenuation range of 0 to –8.5 dB. This adjusting starts at the RinL/A input level of –24 dBm0.
1: Gain control function ON
0: Gain control function OFF

(10) CR9 (Setting of acoustic echo canceler operating mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR9	ATHR	ADCL	ACCL	AHD	ACLP (NLP)*1	AHLD (ADP)*1	AATT (ATT)*1	AGC (GC)*1
Initial value	1	0	0	0	0	0	0	0

*1 Name of a control pin used by the MSM7602

B7 … Through mode control bit for acoustic echo canceler.
In this mode, RinA data and SinA data is output directly to RoutL and SoutL respectively. The coefficient is not cleared.
1: Through mode 0: Normal mode (echo cancellation)

B6 … Selects whether or not to clear the coefficient 1 of the adaptive FIR filter (AAFF) for the acoustic echo canceler.
1: Resets the coefficient 0: Normal operation

B5 … Selects whether or not to clear the coefficient 2 of the adaptive FIR filter (AAFF) for the acoustic echo canceler.
1: Resets the coefficient 0: Normal operation

B4 … Howling detector (HD) ON/OFF control 1: ON 0: OFF

B3 … Turns ON or OFF the Center Clipping function which forcibly sets the Sout output of the acoustic echo canceler to a minimum positive value when it is –57 dBm0 or less.
1: Center Clipping ON
2: Center Clipping OFF

B2 … Selects whether or not to update the coefficient of the adaptive FIR filter (AAFF) for the acoustic echo canceler.
1: Coefficient fixed mode
0: Normal mode (updates the coefficient.)

B1 … Turns ON or OFF the ATT function which prevents howling from occurring by means of attenuators ATTrA and ATTsA provided for the RinA input and the SoutA output of the acoustic echo canceler.
When a signal is input to RinA only, the attenuator ATTsA of the SoutA output is activated. When a signal is input to SinA only or to both SinA and RinA, the attenuator ATTrA of the RinA input is activated. Their ATT values are both about 6 dB.
1: ATT function OFF
0: ATT function ON

B0 … Turns ON or OFF the gain control function which controls the RinA input level and prevents howling from occurring by the gain controller (GainA) for the RinA input of the acoustic echo canceler.
The RinL/A input level is adjusted in the attenuation range of 0 to –8.5 dB. This adjusting starts at the RinL/A input level of –24 dBm0.
1: Gain control ON
0: Gain control OFF

(11) CR10 (Tone detection frequency)

	B7	B6	B5	B4	B3	B2	B1	B0
CR10	—	—	—	DMWR	D TONE3	D TONE2	D TONE1	D TONE0
Initial value	0	0	0	0	0	0	0	0

B7, 6, 5... Not used

B4... Controls changing the default value in default store memory
1: Write
Writes the 16-bit data that is set in CR15 (D15-D8) and CR16 (D7-D0) into the 16-bit addresses that are set in CR13 (A15-A8) and CR14 (A7-A0)

B3, 2, 1, 0 ... Reserved

(12) CR11 (Transmit side pad control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR11	LATTL2	LATTL1	LATTL0	LATTG2	LATTG1	LATTG0	—	—
Initial value	0	0	0	0	0	0	0	0

B7, 6, 5... Setting of pad for transmit loss
(0, 0, 0) : 0 dB
(0, 0, 1) : –2 dB
(0, 1, 0) : –4 dB
(0, 1, 1) : –6 dB
(1, 0, 0) : –8 dB
(1, 0, 1) : –10 dB
(1, 1, 0) : –12 dB
(1, 1, 1) : –14 dB

B4, 3, 2... Setting of pad for transmit gain
(0, 0, 0) : 0 dB
(0, 0, 1) : 2 dB
(0, 1, 0) : 4 dB
(0, 1, 1) : 6 dB
(1, 0, 0) : 8 dB
(1, 0, 1) : 10 dB
(1, 1, 0) : 12 dB
(1, 1, 1) : 14 dB

(13) CR12 (Receive side pad control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR12	AATTL2	AATTL1	AATTL0	AATTG2	AATTG1	AATTG0	—	—
Initial value	0	0	0	0	0	0	0	0

B7, 6, 5... Setting of pad for receive loss
(0, 0, 0) : 0 dB
(0, 0, 1) : –2 dB
(0, 1, 0) : –4 dB
(0, 1, 1) : –6 dB
(1, 0, 0) : –8 dB
(1, 0, 1) : –10 dB
(1, 1, 0) : –12 dB
(1, 1, 1) : –14 dB

B4, 3, 2... Setting of pad for receive gain
(0, 0, 0) : 0 dB
(0, 0, 1) : 2 dB
(0, 1, 0) : 4 dB
(0, 1, 1) : 6 dB
(1, 0, 0) : 8 dB
(1, 0, 1) : 10 dB
(1, 1, 0) : 12 dB
(1, 1, 1) : 14 dB

(14) CR13, 14, 15, 16 (Default value store registers)

	B7	B6	B5	B4	B3	B2	B1	B0
CR13	A15	A14	A13	A12	A11	A10	A9	A8
Initial value	0	0	0	0	0	0	0	0

	B7	B6	B5	B4	B3	B2	B1	B0
CR14	A7	A6	A5	A4	A3	A2	A1	A0
Initial value	0	0	0	0	0	0	0	0

	B7	B6	B5	B4	B3	B2	B1	B0
CR15	D15	D14	D13	D12	D11	D10	D9	D8
Initial value	0	0	0	0	0	0	0	0

	B7	B6	B5	B4	B3	B2	B1	B0
CR16	D7	D6	D5	D4	D3	D2	D1	D0
Initial value	0	0	0	0	0	0	0	0

Direct Access to Default Store Memory

The contents of the default store memory can be changed (e.g., to change tone detection levels and tone generation frequencies) in the initial mode (CR0-B3 to CR0-B0="0000").
Refer to the following procedure:

- Set the default value store memory address (CR13, CR14).
- Set the write data into CR15 and CR16.
- Set the DMWR (change default) command (CR10-B4="1").

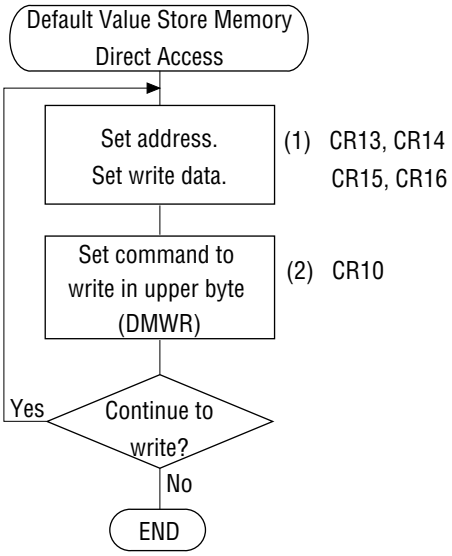


Figure 8 Flow Chart of Default Value Store Memory Direct Access

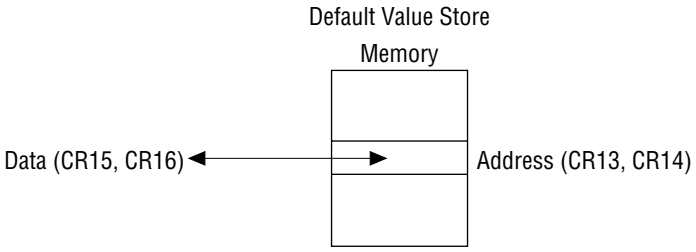


Figure 7 Memory Map for Default Value Store Memory Direct Access

Resetting of Echo Canceler Coefficient

In cases where an echo path changes, the echo canceler may be slow in converging. In such cases, resetting the coefficient of the echo canceler can force it to converge immediately.
In addtion, if the echo path changes after the coefficient is reset, the echo canceler may again be slow in converging.
There are four resetting modes available, as shown in the table below. If an echo path changes, execute coefficient reset both by $\overline{\text{LDCL}}/\overline{\text{ADCL}}$ and by $\overline{\text{LCCL}}/\overline{\text{ACCL}}$ pin control (Reset 3) whenever possible, because resetting by both of them do not affect any echo path state.

Control	Echo Convergence Time	Degree of Effect on Echo Route
No reset (LTHR/ATHR)	Fast	Significant
Reset 1 ($\overline{\text{LDCL}}/\overline{\text{ADCL}}$)		
Reset 2 ($\overline{\text{LCCL}}/\overline{\text{ACCL}}$)		
Reset 3 (both $\overline{\text{LDCL}}/\overline{\text{ADCL}}$ and $\overline{\text{LCCL}}/\overline{\text{ACCL}}$)	Slow	No effect

Notes on Data Communication

Use the following setting when making data communication:

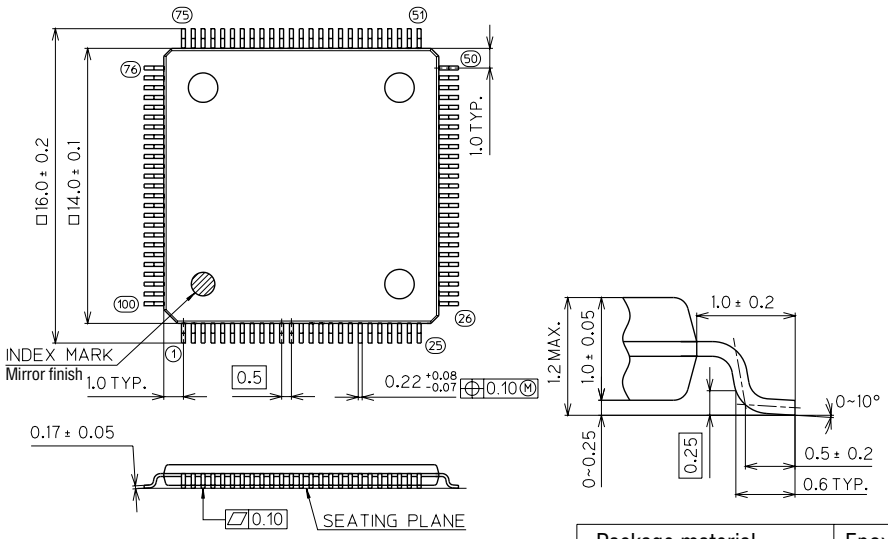
For 4-bit (32 kbps) data communication:
DTHR="1" (common to handsfree communication mode and line echo canceler expansion mode)

Notes:
1. The MSM7719 does not support 8-bit (64 kbps) data communication.
2. Data dropouts or a data error of a few SYNCs occurs upon switching between data communication and voice communication.
3. Of the voice data through modes, ATHR and LTHR converts PCM data "7Fh" into "FFh".

PACKAGE DIMENSIONS

(Unit : mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.55 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).